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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,884	02/13/2002	Krishnaswamy Ramkumar	5298-08000 PM01040	6510

35617 7590 06/18/2003

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P.O. BOX 684908  
AUSTIN, TX 78768

EXAMINER
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ERDEM, FAZLI

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/074,884

Applicant(s)

RAMKUMAR

Examiner

Fazli Erdem

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 12, 16, 17, 19 and 22 is/are rejected.
- 7) ☒ Claim(s) 9-11, 13-15, 18, 20, 21 and 23-25 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

NATHAN J. FLYNN

SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

**DETAILED ACTION**

***Allowable Subject Matter***

1. Claims 9-11, 13-15, 18, 20, 21, 23-25 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Hodges (6,040,233) in view of Freiburger (5,104,819) further in view of Buchanan et al. (6,245,616) further in view of Lin et al. (5,930,625).

Regarding Claims 1-8, Hodges discloses a method of making a shallow trench isolation with thin nitride as gate dielectric where a semiconductor structure comprises a silicon substrate of a first conductivity type including wells of a second conductivity type disposed on a surface thereof and a dielectric layer including silicon nitride disposed on the surface. The dielectric layer includes openings at least partially disposed on the p-wells. The dielectric layer also includes a top layer comprising silicon dioxide having a thickness of less than ten angstroms. Trenches having a depth comparable to or greater than a depth of the wells extend into the

substrate surface within the openings. A nonconductive material is disposed within the trenches and has an upper surface that is substantially coplanar with the dielectric layer. Portions of the dielectric layer are used as gate dielectric for transistors. Hodges fails to disclose the required capacitance, gate dielectric and gate dielectric with proper thickness structures. However, Buchanan et al. disclose a method of forming oxynitride gate dielectric where the required capacitance structure is disclosed. Furthermore, Lin et al. disclose a method for fabricating a stacked or crown chaped capacitor structure where the required capacitance the required gate dielectric structure is disclosed. Finally, Freiburger et al. disclose a fabrication of interpoly dielectric for EPROM related technologies where the required gate dielectric with the proper thickness is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required capacitance, gate dielectric and gate dielectric with proper thickness structures as taught by Buchanan et al., Lin et al., and Freiburger et al. respectively in order to have a semiconductor insulating/dielectric layer with better performance.

3. Claims 12, 16, 17, 19 and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Shue et al. (6,380,056) in view of Krussel et al. (5,304,398) further in view of Tremont et al. (4,749,640).

Regarding Claims 12, 16, 17, 19 and 22, Shue et al. disclose a lightly nitridation surface for preparing thin-gate oxides where a method for forming a dielectric layer upon a silicon layer is disclosed. There is first provided a substrate employed within a microelectronics fabrication. Then a silicon layer formed over the substrate. There is then formed through use of a first

thermal annealing method employing a nitrogen containing annealing atmosphere in absence of an oxidizing material or a reducing material silicon nitride containing layer upon a partially consumed silicon layer derived from the silicon layer. There is then oxidized through use of a second thermal annealing method employing an oxidizing material containing atmosphere the silicon nitride containing layer to form an oxidized silicon nitride containing layer upon a further consumed silicon layer derived from the partially consumed silicon layer. Shue et al. fail to disclose the ozonation method and ozonated substance structures. However, Tremont et al. disclose integrated circuit manufacturing process where the required ozonation method is disclosed. Furthermore, Krusell et al. disclose a chemical vapor deposition of silicon dioxide using hexamethyldisilazane where the required ozonated substance is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required ozonation method and the ozonated substance in Shue et al. as taught by Tremont et al. and Krusell et al. respectively in order to make a semiconductor dielectric/insulating substrate with better performance.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

FE  
June 16, 2003